IN THE SPECIFICATION:

(1) The paragraph from page 1, line 21 to line 30 has been amended as follows:

In general, in a semiconductor test device, a test pattern signal is input into a semiconductor device (device under test: DUT) which is a test object, a response signal output from the DUT is compared with an expected pattern signal to judge agreement/disagreement, and accordingly the DUT is tested. Moreover, the semiconductor test device usually comprises includes a timing generation circuit (TG) which generates a timing of a waveform to be applied to the DUT in order to apply a test signal to the DUT at a predetermined timing.

(2) The paragraph from page 2, line 4 to line 9 has been amended as follows:

As shown in the figure FIG. 10, the memory test device comprises includes: a timing generation circuit (timing generator: TG) 1; a pattern generation unit 2; a waveform formatter 3; a logical comparison unit 4; and a failure analysis memory unit 5, and constitutes thereby constituting a memory test device for testing a memory M to be tested.

(3) The paragraph from page 2, line 4 to line 9 has been amended as follows:

The pattern generation unit 2 generates an address signal to be applied to the memory M to be tested which is a test object, test pattern data, control signal, and an expected

value data to be applied to the logical comparison unit 4 in accordance with the reference clock generated by the timing generation circuit 1.

(4) The paragraph from page 2, line 29 to page 3, line 4 has been amended as follows:

On inputting the response signal from the memory M to be tested, and the expected value data generated by the pattern generation unit 2, the logical comparison unit 4 compares both the data to detect the agreement/disagreement. Accordingly, it is judged whether or not a test the memory 110 M under test is satisfactory.

(5) The paragraph from page 3, line 5 to page 3, line 12 has been amended as follows:

Fail data is inputted into the failure analysis memory unit 5 in a case where the response signal from the memory M to be tested disagrees with the expected value data. The fail data is stored in a memory cell corresponding to the address signal output from the pattern generation unit 2. The fail data stored in the failure analysis memory unit 5 is separately read out and used in analyzing a predetermined the failure of the memory M.

- (6) The paragraph from page 3, line 14 to page 3, line 16 has been amended as follows:
 - FIG. 11 is a block diagram showing details of a conventional timing generation circuit disposed incorporated in the semiconductor test device described above.

(7) The paragraph from page 3, line 25 to page 4, line 1 has been amended as follows:

In this conventional timing generation circuit, the timing data stored in the timing memory 110 is set in the down counter 120, and the set timing data is loaded by the load signal of the counter load enable selection circuit 130 to thereby make a decrement the timing data by one in synchronization with each occurrence of a CLK signal in the down counter 120.

(8) The paragraph from page 4, line 7 to page 4, line 19 has been amended as follows:

Specifically, to operate the timing generation circuit actually in the semiconductor test device, any one of column-direction addresses (Adr: 0 to Adr: n-1 shown in FIG. 11) of a TMM 10 the TMM 110 is designated, accordingly the data of a row-direction bit width (m bits b0 to bm-1 in an example shown in FIG. 11) stored in the address is set in the a down counter 20, and timing data can be loaded by the load signal of the counter load enable selection circuit 130 to count down. Thus, in the conventional timing generation circuit, when the timing data indicating a desired timing is stored in the TMM, for example, a timing signal can be generated which is indicated by a delay time which is an arbitrary integer times multiple of a CLK signal period.

(9) The paragraph from page 5, line 4 to page 5, line 15 has been amended as follows:

However, in the conventional timing generation circuit in which a delay amount (e.g., 16 µs or less with a 20-bit width, etc.) is determined by the bit width (row direction) of the TMM in this manner, in order to handle a longer delay amount, it is necessary that a memory configuration of the TMM is changed, and the row-direction bit width is added. Moreover, it has been necessary to add a bit number per phase of the next-stage down counter. Therefore, to lengthen increase the delay amount, a circuit scale of the timing edge generation unit enormously increases, and a problem has occurred that the cost of a gate array cost increases in for establishing the timing generation circuit significantly increases.

(10) The paragraph from page 5, line 20 to page 5, line 29 has been amended as follows:

The present invention has been proposed to solve the problem of above-noted problems involved in the conventional art, and an object is to provide a timing generation circuit which is capable of increasing a maximum delay amount or as well as increasing a timing set number without changing a configuration of a timing memory containing timing data and which realizes a several types of TGs by one type of hardware configuration and in which enables low-cost device measurement is possible, and. Another object of the present invention is semiconductor to provide а test device comprising incorporating this timing generation circuit.